

CLAIMS

1. A method for amortizing a critical path computations in a circuit comprising:

5 unrolling a data flow graph representing said circuit into a plurality of clock cycles; and
simulating said circuit in said plurality of clock cycles on a computer.

2. The method of claim 1, wherein said step of simulating further comprises:
reducing a difference between said critical path and a shortest path in said data flow

10 graph.

3. The method of claim 2, wherein said step of reducing further comprises:
compacting one or more computations from said plurality of clock cycles in a processor.

15 4. The method of claim 2, wherein said step of unrolling further comprises:
eliminating one or more flip-flops between one or more boundaries within said plurality
of clock cycles.

5. The method of claim 2, wherein said step of unrolling further comprises:
20 eliminating one or more latches between one or more boundaries within said plurality of
clock cycles.

6. The method of claim 1, wherein said computer has a plurality of processors.

7. The method of claim 1, wherein said computer has a plurality of simulation processors, wherein said simulation processors include a communication network interconnecting said simulation processors for data communication, said simulation processors further including a synchronization network interconnecting said simulation processors for
5 synchronizing execution therebetween.

8. The method of claim 1, wherein said step of simulating further comprises:
delaying evaluation of one or more logic elements within said plurality of clock cycles,
thereby creating a timing slack for inter-processor communication.

9. The method of claim 3, wherein said step of reducing further comprises:
using a first processor wherein said processor computes said critical path and a non-
critical path in a said plurality of clock cycles.

10. The method of claim 1, further comprising:
compacting said plurality of clock cycles into a single clock cycle.

11. A critical path computation amortizer for a circuit comprising:
a data flow graph unroller configured to represent said circuit into a plurality of clock
20 cycles; and
a simulator configured to simulate said circuit in said plurality of clock cycles on a
computer.

12. The critical path computation amortizer of claim 11, wherein said simulator
25 further comprises:

a reducer configured to reduce a difference between said critical path and said shortest path.

13. The critical path computation amortizer of claim 12, wherein said reducer further
5 comprises:

a compactor configured to compact one or more computations from said plurality of clock cycles in a processor.

14. The critical path computation amortizer of claim 12, wherein said unroller
10 further comprises:

an eliminator configured to eliminate one or more flip-flops at one or more boundaries within said plurality of clock cycles.

15. The critical path computation amortizer of claim 12, wherein said unroller
15 further comprises:

an eliminator configured to eliminate one or more latches at one or more boundaries within said plurality of clock cycles.

16. The critical path computation amortizer 11, wherein said computer has a
20 plurality of processors.

17. The critical path computation amortizer of claim 11, wherein said computer has a plurality of simulation processors, wherein said simulation processors include a communication network interconnecting said simulation processors for data communication, said simulation

processors further including a synchronization network interconnecting said simulation processors for synchronizing execution therebetween.

18. The critical path computation amortizer of claim 11, wherein said simulator is
5 further configured to delay evaluation of one or more logic elements in said plurality of clock cycles, thereby creating a timing slack for inter-processor communication.

19. The critical path computation amortizer of claim 13, wherein said reducer further comprises:

10 a feed-back configured to use a first processor wherein, said first processor computes said critical path and a non-critical path in said plurality of clock cycles.

20. The critical path computation amortizer of claim 11, further comprising:
a scheduling compactor configured to compact said plurality of clock cycles into a single clock cycle.

21. A computer program product comprising:
a computer usable medium having computer readable program code embodied therein configured to amortize a critical path computation in a circuit, said computer program product comprising:

15 computer readable code configured to cause a computer to unroll a data flow graph representing said circuit into a plurality of clock cycles; and

computer readable code configured to cause a computer to simulate said circuit in said plurality of clock cycles on a computer.

22. The computer program product of claim 21, wherein said computer readable code configured to cause a computer to simulate further comprises:

computer readable code configured to cause a computer to reduce a difference between said critical path and said shortest path.

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23. The computer program product of claim 22, wherein said computer readable code configured to cause a computer to reduce further comprises:

computer readable code configured to cause a computer to compact one or more computations from said plurality of clock cycles in a processor.

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24. The computer program product of claim 12, wherein said computer readable code configured to cause a computer to unroll further comprises:

computer readable code configured to cause a computer to eliminate one or more flip-flops at one or more boundaries within said plurality of clock cycles.

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25. The computer program product of claim 12, wherein said computer readable code configured to cause a computer to unroll further comprises:

computer readable code configured to cause a computer to eliminate one or more latches at one or more boundaries within said plurality of clock cycles.

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26. The computer program product of claim 21, wherein said computer has a plurality of processors.

27. The computer program product of claim 21, wherein said computer has a plurality of simulation processors, wherein said simulation processors include a communication

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network interconnecting said simulation processors for data communication, said simulation processors further including a synchronization network interconnecting said simulation processors for synchronizing execution therebetween.

5 28. The computer program product of claim 21, wherein said computer readable code configured to cause a computer to simulate further comprises:

computer readable code configured to cause a computer to delay evaluation of one or more logic elements in said plurality of clock cycles, thereby creating a timing slack for inter-processor communication.

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29. The computer program product of claim 20, wherein said computer readable code configured to cause a computer to reduce further comprises:

computer readable code configured to cause a computer to use a first processor wherein said first processor computes said critical path and a non-critical path in said plurality of clock cycles.

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30. The computer program product of claim 21, further comprising:

computer readable code configured to cause a computer to compact said plurality of clock cycles into a single clock cycle.